



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

10/813,794

03/31/2004

Raymond Scott Tetrick

30320/17862

7546

4743 7590 02/19/2008
MARSHALL, GERSTEIN & BORUN LLP
233 S. WACKER DRIVE, SUITE 6300
SEARS TOWER
CHICAGO, IL 60606

EXAMINER

KAWSAR, ABDULLAH AL

ART UNIT

PAPER NUMBER

2195

MAIL DATE

DELIVERY MODE

02/19/2008

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

AK

Office Action Summary	Application No. 10/813,794	Applicant(s) TETRICK, RAYMOND SCOTT	
	Examiner ABDULLAH AL KAWSAR	Art Unit 2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 31 March 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-26 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-26 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 03/31/2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Claims 1-26 are rejected.

Claim Objections

2. Claims 22-26 objected to because of the following informalities: claims disclose "computer readable memory" which was not described in the specification of the application. The specification reads "computer accessible medium" which includes tangible (e.g. ROM, RAM, flash drive, magnetic disk) media and non-tangible (e.g. carrier waves, infrared signals, and digital signals) which introduces possible 101 problems. Applicant is suggested to amend the claims and include only the tangible medium. Appropriate correction is required.

Claim Rejections - 35 USC § 101

3. 35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

4. Claims 1-21 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Claims 1 and 17 are non-statutory as they fail to produce a "useful, concrete and tangible result". The claim steps do not accomplish the result claimed in the pre-amble of the claim.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1-26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

- a. The following claims languages are not clearly understood:
 - i. Claim 1, line 1 recites "reserving an execution thread" it is unclear what is meant by that. Line 2 recites "describing" and "processing unit as peripheral device" it is unclear where it is being described and how it is being described (i.e. describing in the BIOS? Creating new boot loader files of device description with different memory address and input/output?) Line 4 recite "preventing peripheral devices" it is unclear how peripheral devices are prevented (i.e. blocking the processing unit? Disabling?).
 - ii. Claims 17 and 22 have similar deficiency as claim 1 above.
 - iii. Claim 2, line 1 recite "reading the device description" it unclear where the device description is being read.
 - iv. Claim 17 has similar deficiency as claim 2 above.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 1-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lai(Lai) US Patent No. 6546483, in view of Stanley(Stanley) US Patent No. 6457069.

9. As per claim 1, Lai teaches a method of reserving an execution thread comprising:
describing a selected processing unit as a peripheral device in a device description (col 2, lines 5-7; lines 61-65; col 3, lines 3-9);

providing a processor description including one or more available processing units to an operating system, wherein the selected processing unit is omitted from the processor description (col 1, lines 56-58; lines 60-65).

10. Lai does not specifically disclose preventing peripheral devices from using the selected processing unit.

11. However, Stanley teaches preventing peripheral devices from using the selected processing unit (col 2, lines 59-63); and

12. It would have been obvious to a person of ordinary skill in art at the time of invention was made to incorporate the teaching of Stanley into the method of Lai to prevent peripheral device from using the selected processing unit. The modification would have been obvious because one of the ordinary skills of the art would have disabled the processing unit being

accessed by other peripheral device to be able to modify the device description for later configuration.

13. As per claim 2, Lai teaches reading the device description of the selected processing unit (col 1, lines 56-60);

recognizing the device description of the processing unit as a device description of a peripheral device (col 2, lines 5-8);

retrieving a device driver for the processing unit based on the device description of the selected processing unit (col 3, lines 3-9); and

allocating resources to the selected processing unit based on a request from the driver (col 3, lines 14-23).

14. As per claim 3, Lai teaches communicating with the processing unit as a peripheral device via the driver (col 1, lines 66-67 through col 2, lines 1-3).

15. As per claim 4, Stanley teaches the device description comprises an identification unique to the selected processing unit (col 9, lines 17-20).

16. As per claim 5, Stanley teaches the device description comprises at least one of the following: vendor identification, device identification, allocated address space, interrupt capabilities, basic input/output system code address and power saving capabilities (col 2, lines 5-9; col 5, lines 20-26).

17. As per claim 6, Lai teaches describing the selected processing unit comprises describing the selected processing unit as a peripheral device in a bus configuration header (col 3, lines 1-9; col 4, lines 32-43).

18. As per claim 7, Lai teaches describing the selected processing unit comprises creating the device description and setting device configuration values for the selected processing unit (col 3, lines 3-9).

19. As per claim 8, Lai teaches describing the selected processing unit comprises describing the selected processing unit as a peripheral device in a device configuration description within a bus configuration space (col 2, lines 49-60; col 3, lines 3-9).

20. As per claim 9, Stanley teaches preventing peripheral devices from using the selected processing unit comprises modifying an interrupt controller to prevent the selected processing unit from receiving interrupt requests (abstract, lines 9-12).

21. As per claim 10, Stanley teaches providing the processor description of one or more available processing units to an operating system comprises providing a power management table to the operating system, wherein the power management table includes a description of all available processing units except the selected processing unit (col 7, lines 15-23).

22. As per claim 11, Stanley enabling a processor to allow the device description to be written and notifying the selected processing unit of the device description (col 8, lines 10-15).

23. As per claim 12, Stanley teaches accessing the selected processing unit from a front side bus and from a processor (col 8, lines 66-67 through col 9, lines 1-4).

24. As per claim 13, Lai teaches executing at least one of the following using the selected processing unit: a system health monitor, an operating system kernel external to the operating system, a device, a system performance enhancement, a network stack partition, and server management (col 2, lines 5-8; col 6, lines 1-11).

25. As per claim 14, Lai and Stanley do not specifically disclose the processing unit comprises a logical processing unit related to one or more execution threads.

26. It would have been obvious to a person of ordinary skill in art at the time of invention was made have a processing unit as logical processing unit related to one of more execution thread to utilize the new architecture of processor with multiple programmable logical units.

27. As per claim 15, Lai and Stanley do not specifically disclose the processing unit comprises a processing core related to one or more execution threads.

28. It would have been obvious to a person of ordinary skill in art at the time of invention was made have a processing unit as logical processing unit related to one of more execution thread to utilize the new architecture of processor with multiple core processing cores.

29. As per claim 16, Lai teaches a basic input/output system program performing the method of claim 1(col 3, lines 10-15).

30. As per claim 17, it has similar limitations as of combined method of claims 1 and 2 above. Therefore, it is rejected under the same rational as of combined method of claims 1 and 2 above.

31. As per claim 18, it has similar limitations as of claim 3 above. Therefore it is rejected under the same rational as of claim 3 above.

32. As per claim 19, it has similar limitations as of combined method of claims 6 and 7 above. Therefore, it is rejected under the same rational as of combined method of claims 6 and 7 above.

33. As per claim 20, Lai teaches reading a description of a processor including one or more available processing units, wherein the processing unit is omitted from the processor description (col 1, lines 56-58; lines 60-65).

34. As per claim 21, Stanley teaches an operating system performing the method of claim 17 (col 7, lines 42-48).

35. As per claims 22-26, they have similar limitations as of claims 1, 6, 7, 9 and 10 above. Therefore, they are rejected under the same rational as of claims 1, 6, 7, 9 and 10 above.

Conclusion

36. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Cooper (US Patent No. 6823516); Bealkowski et al. (US Patent No. 6282596);

37. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Abdullah-Al Kawsar whose telephone number is 571-270-3169. The examiner can normally be reached on 7:30am to 5:00pm, EST.

38. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng Ai T. An can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Application/Control Number:
10/813,794
Art Unit: 2195

Page 10

39. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Abdullah Al Kawsar
Patent Examiner
Art Unit 2195.


MENG-FU T. AN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100